

## Course 304

# x86-32, Intel64 and AMD64 CPU Architectures From the '386 to Core i7 and Phenom

## A 3-day Course

This course provides a detailed description of the latest Intel and AMD 32/64-bit processor architectures and their implementations in *Core 2*, *Core i7*, *Xeon*, *Athlon*, *Opteron*, and *Phenom* processors. While the primary focus is on the current *Core i7* and *Phenom* processors other members of the families are also reviewed. Key features and characteristics of Intel and AMD chipsets designed to support the different versions are covered as well as the details of system implementation from both a hardware and software point of view.

### You will benefit from this workshop if you

- Are designing, validating, or testing state-of-the-art 32/64-bit processors for future products
- Evaluating high-end desktop, workstation, or server systems
- Develop software for Intel and/or AMD based systems
- Want to keep up-to-date with the latest features and capabilities of Intel's and AMD's most widely used processors

### You will learn

- The details of the different Intel and AMD micro-architectures, including instruction processing, pipelining, execution enhancement schemes and cache structure
- The differences between the processors that use the cores, and their impact on PC performance and capabilities
- The features and capabilities of different chipsets that support these architectures
- How processor differences impact PC motherboard layout and power requirements

### Prerequisites

This course is intended for hardware and software design, validation, and test engineers developing single or multi-core Intel or AMD based PCs and servers, as well as project engineers responsible for overseeing or troubleshooting systems that contain advanced 32/64-bit processors.

### The training approach

- **Up to date information:** We update the materials before every event.
- **Straightforward explanations:** Technical concepts and terms are explained in English. You will walk away with a thorough understanding of what the current architectures bring to the table and how to exploit these capabilities.

## Workshop topics

### The Big Picture

- Backward compatibility – The industry’s biggest ongoing challenge
- Legacies from 16-bit processors
- Legacies from early 32-bit processors
- Intel P6 architecture features
- *Core 2* and *Core i7* architectural enhancements
- AMD’s approach

### The Starting Point – The P6 Architecture

- Three-segment pipeline
- Instruction dispersal
- Dynamic execution
- Execution units
- Branch prediction
- Code optimization
- Integer, floating point, and Boolean instructions
- MMX and SSE
- Processor caches
- System bus - FSB
- Multiprocessor systems
- Snooping
- Processor power conservation modes

### Netburst Enhancements That Survived

- SSE2 and SSE3 – More SIMD instructions
- 128-bit integer and floating point operations
- Advanced dynamic execution
- Other execution enhancement schemes

### The Core Architecture

- The P6, *Pentium M*, and Netburst heritage
- Wide dynamic execution
- Instruction decoding
- Instruction fusion
- Branch prediction
- *Core*'s pipeline
- Vector execution units
- Advanced smart cache architecture
- The *Core 2* and *Core i7* processors

### **AMD's Approach**

- Integrated memory controller
- HyperTransport links
- Imitation is the greatest form of flattery – Intel's version for *Core i7* and beyond

### **Chipsets**

- Hub architecture
  - Bus speeds and widths
  - Intel's MCH memory support
  - ICH features
  - Super I/O
  - FWH
  - Current products
- Bridge architecture
  - Northbridge
  - Southbridge
  - Other, specialized components

### **Putting the Processors to Work**

- PC performance history... and predictions
- Motherboard layout
- Power density and power supplies
- Multi-processor configurations
- Over clocking the processor
- Software considerations